Complete Characterization of Backplane Differential Channels

September 16, 2003

presented by:

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Overview

- Backplanes
- Measurement set up
- Single-ended
- Differential
- Frequency & time domain
- Eye diagrams
- Model extraction

All Next Generation High Speed Serial Links will use Differential Signaling

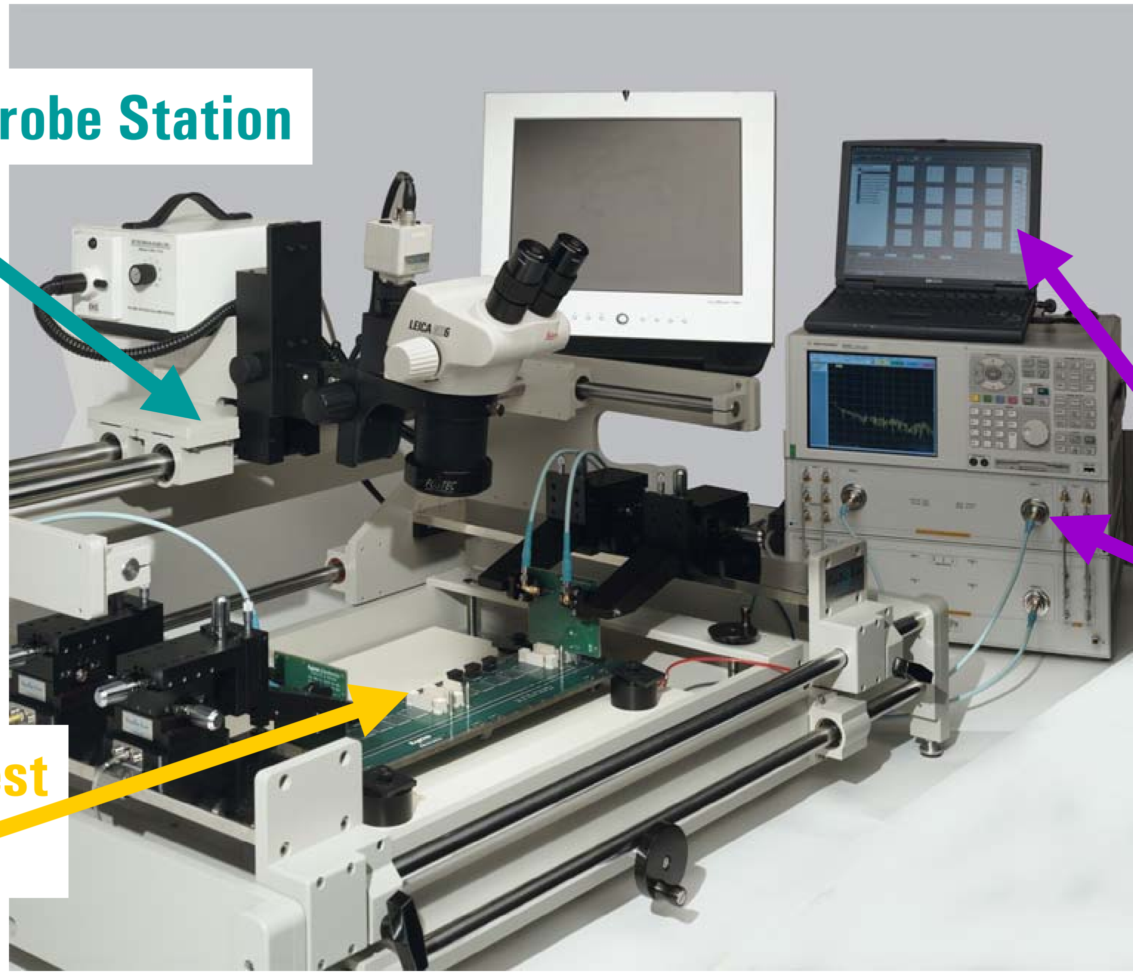
Serial ATA	1.25 Gbps
Hypertransport	1.6 Gbps
AGP8x	2.1 Gbps
Infiniband	2.5 Gbps
PCI Express	2.5 Gbps
Serial ATA II	2.5 Gbps
XAUI	3.125 Gbps
PCI Express II	5.0 Gbps
OC-192	9.953 Gbps
10 GbE	10 Gbps
OC-768	39.81 Gbps

Important Physical Layer Properties of Differential Channels

- Differential impedance profile (diff return loss)
- Transmitted differential signal quality (diff insertion loss)
- Conversion of differential to common signal
- Where conversion of differential to common signal occurs
- Eye diagrams (1 Gbps → 10 Gbps)

Measurement System for Complete Physical Layer Characterization

GigaTest Labs Probe Station

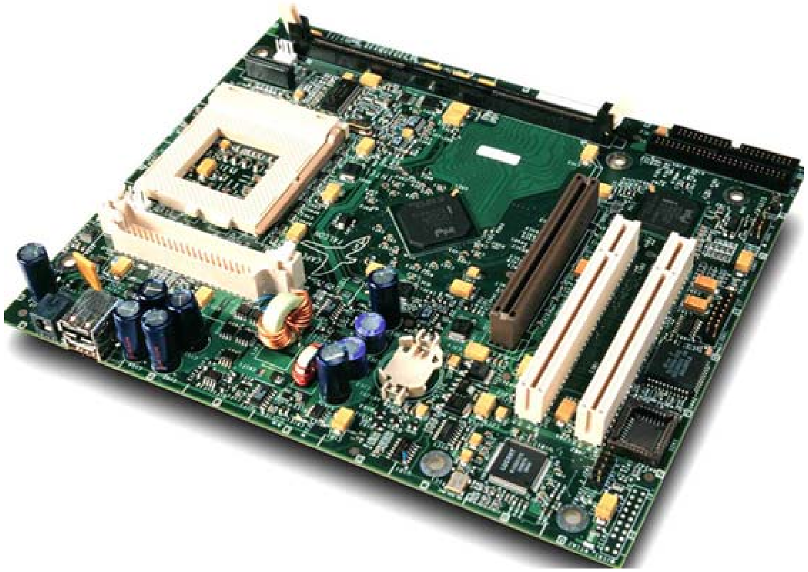


Device Under Test (backplane)

Agilent Physical Layer Test System

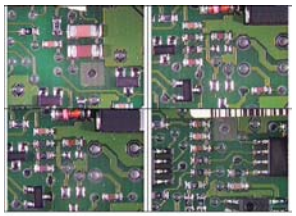
Differential VNA/TDR Applied to All Passive, Linear Components and Interconnects

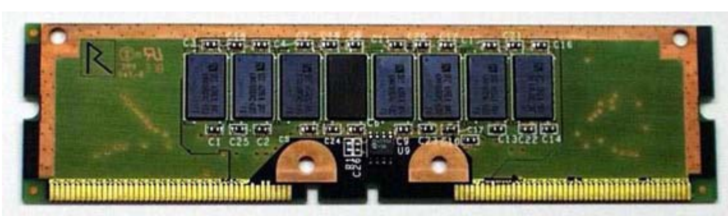
- When an external precision signal is required
- Applies to any passive interconnect or component
  - Backplanes
  - Discretes
  - Packages
  - Connectors
  - PCB structures
  - Material properties

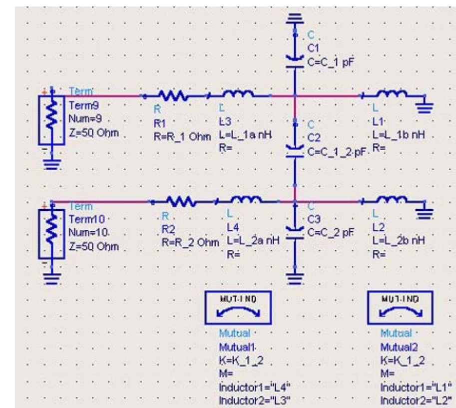


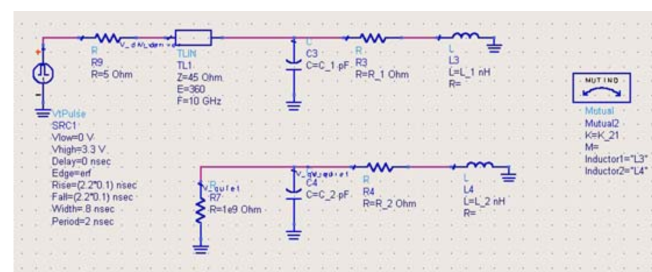
A Precision Instrument is Not Enough!

Component to characterize –?→ **Instrument** –?→ **Valuable information**

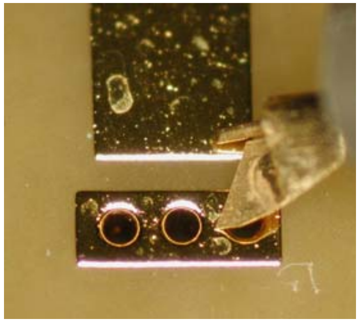




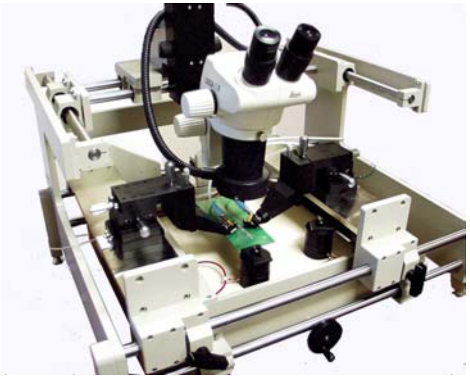




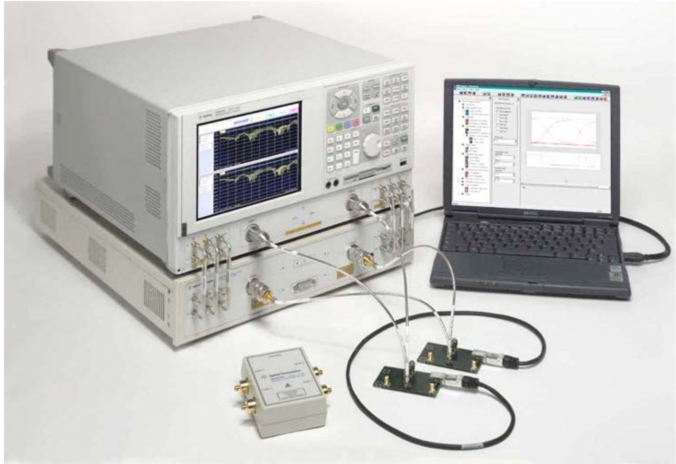
Complete Characterization System Solution



DUT +
microprobes



GigaTest Probe
Station



Physical Layer Test System:
VNA + PLTS software

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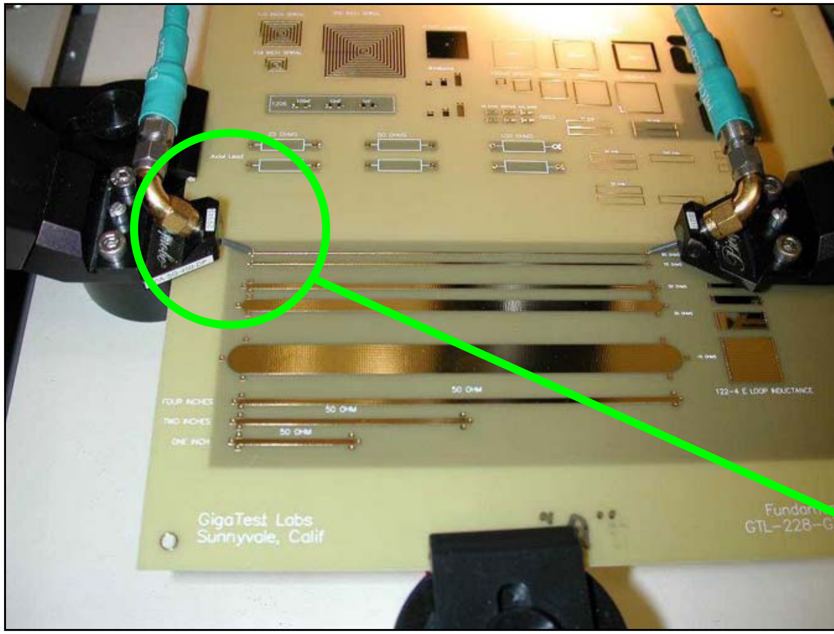
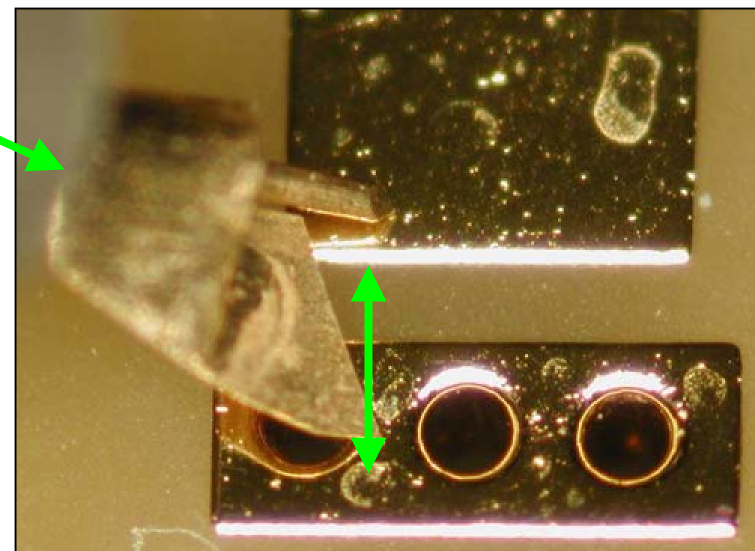
Microprobes Allow Precision Probing of Structures with Minimal Artifacts

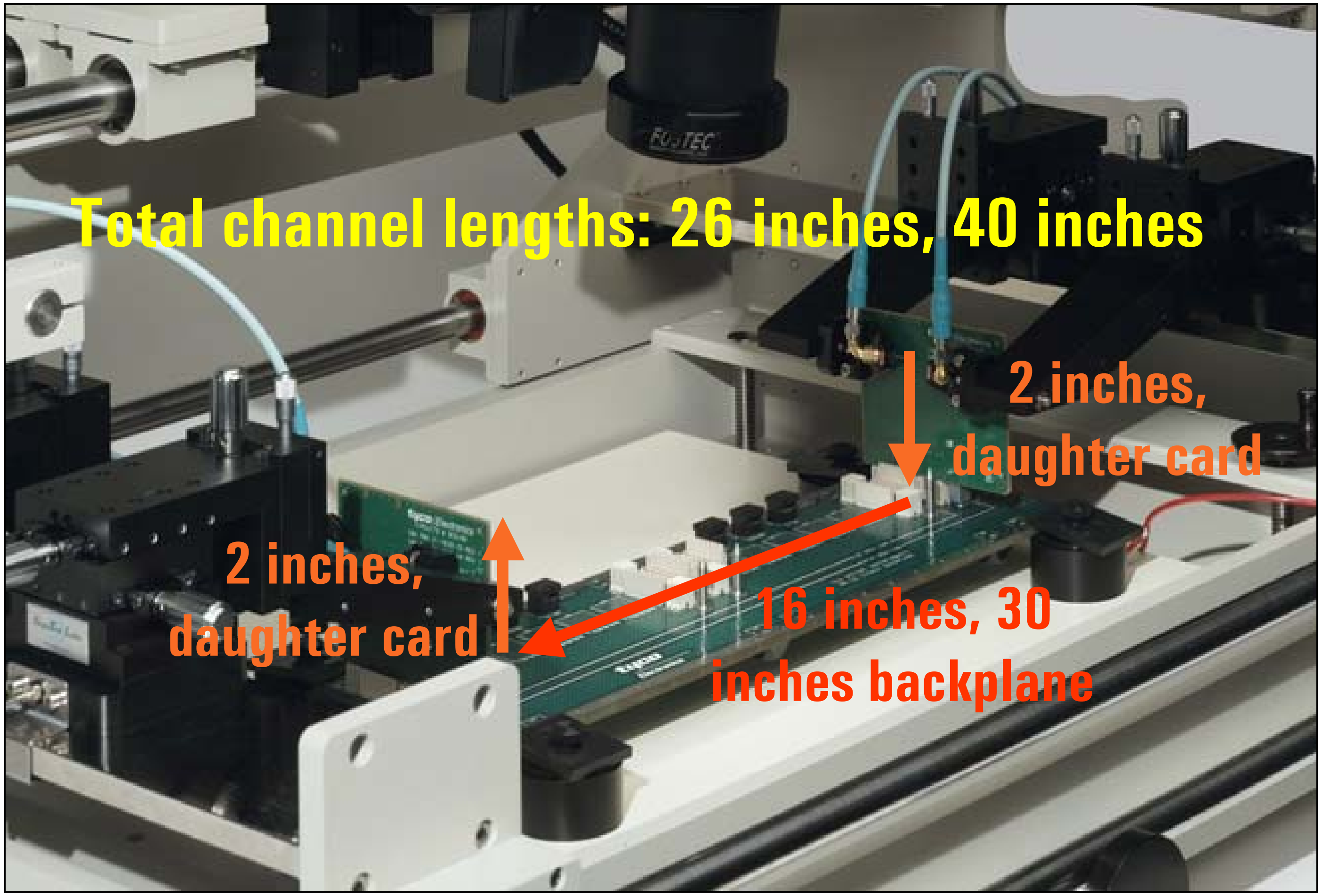


Close up

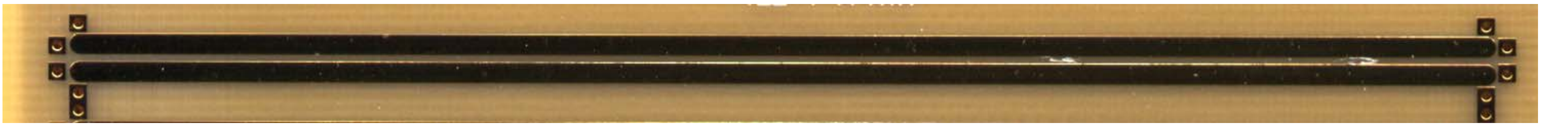


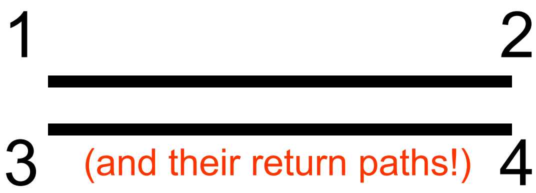
Pitch ~ 50μ – 1000μ

4 Port Differential VNA Techniques Applied to Tyco Electronics HM-Zd Legacy Backplane System



4 Port Single-ended S-parameters





$$S_{out,in} = \frac{P_{out}}{P_{in}}$$

Stimulus

Response				
	S_{11}	S_{12}	S_{13}	S_{14}
	S_{21}	S_{22}	S_{23}	S_{24}
	S_{31}	S_{32}	S_{33}	S_{34}
	S_{41}	S_{42}	S_{43}	S_{44}

Interpreting single ended measurements:

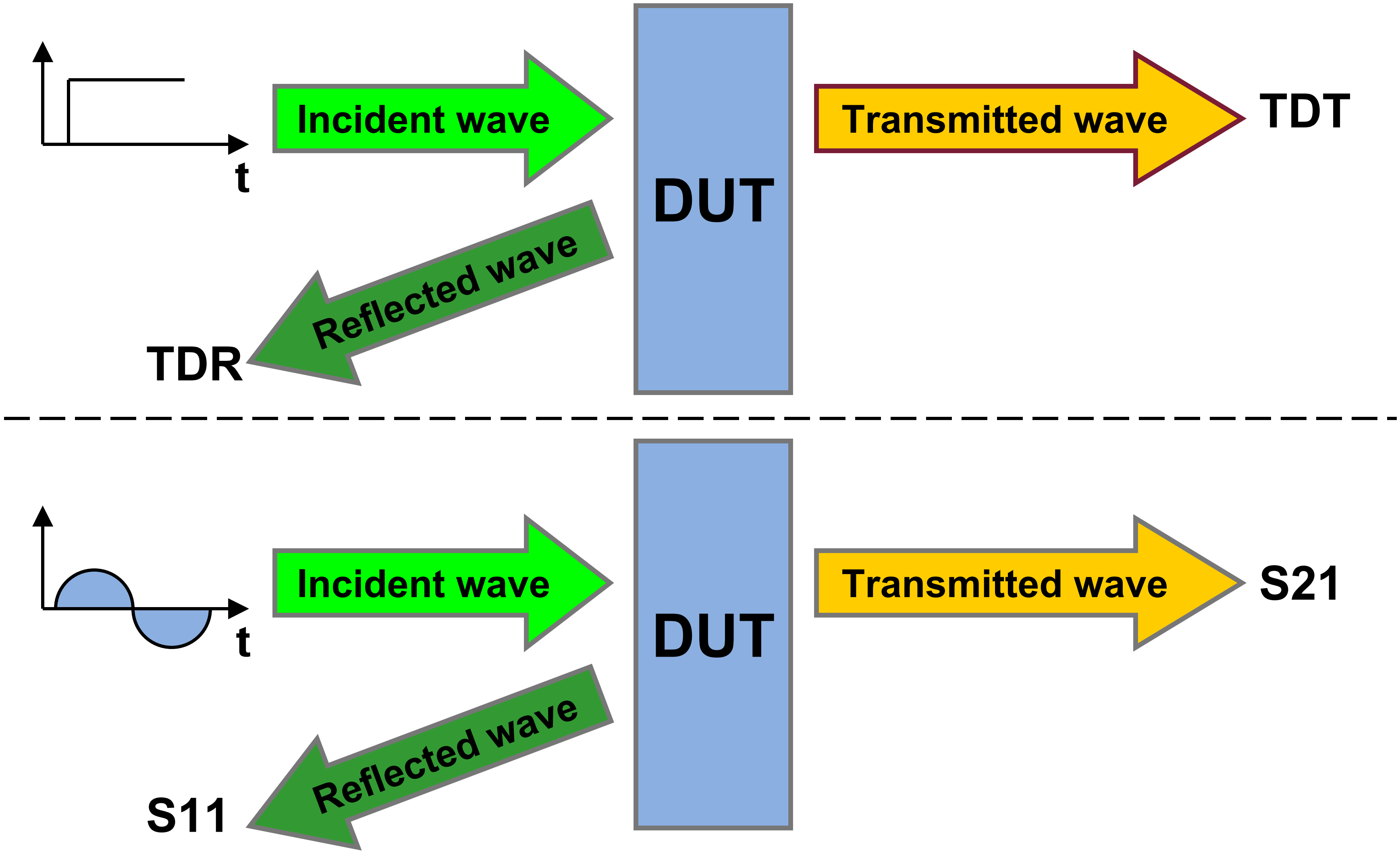
S_{11} : return loss, single ended

$S_{21} = S_{12}$: insertion loss, single ended

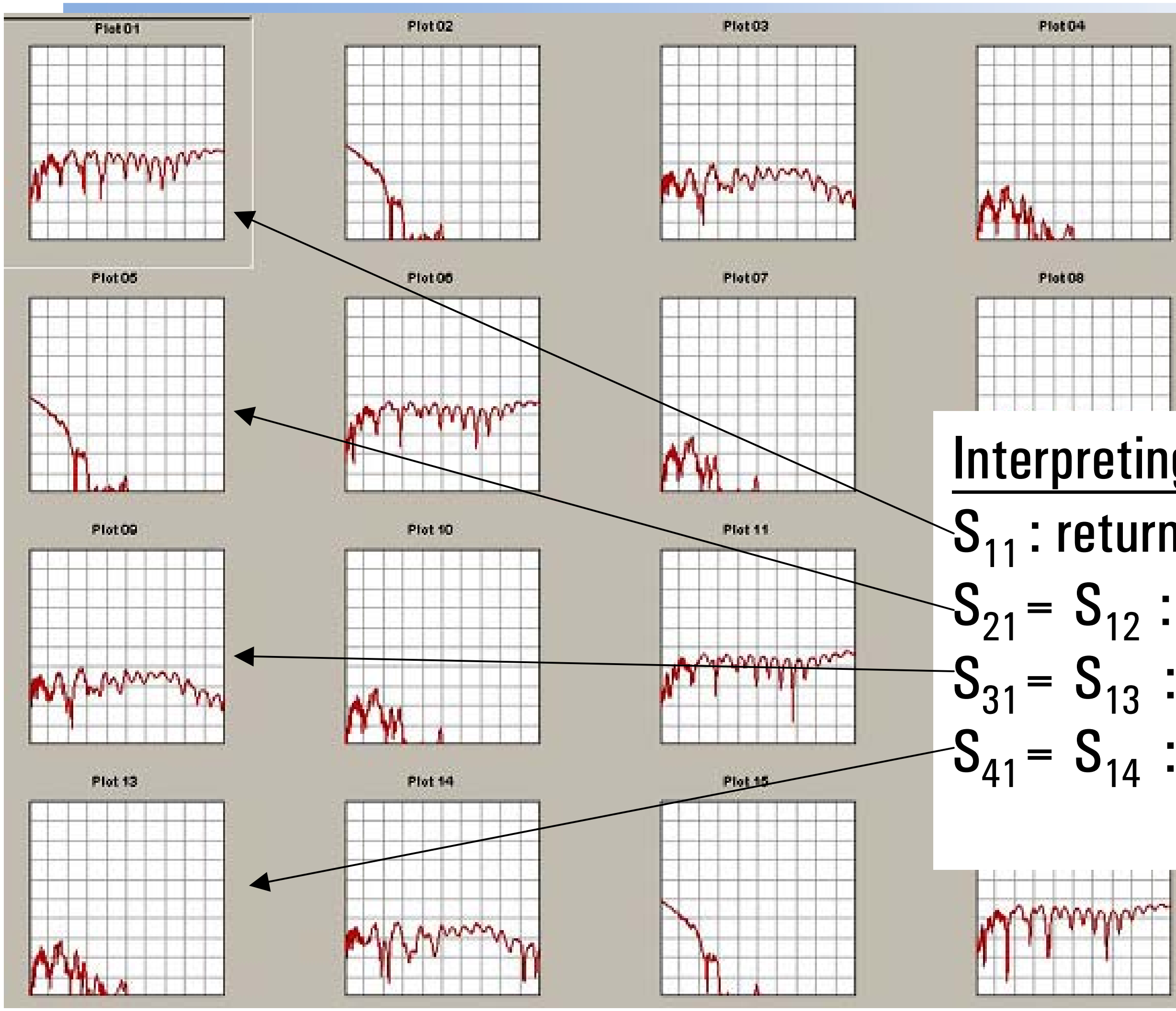
$S_{31} = S_{13}$: near end cross talk

$S_{41} = S_{14}$: far end cross talk

TDR and VNA Techniques



4 Port, Single-ended S-parameters: Tyco Backplane Example



Interpreting single ended measurements:

S_{11} : return loss, single ended

$S_{21} = S_{12}$: insertion loss, single ended

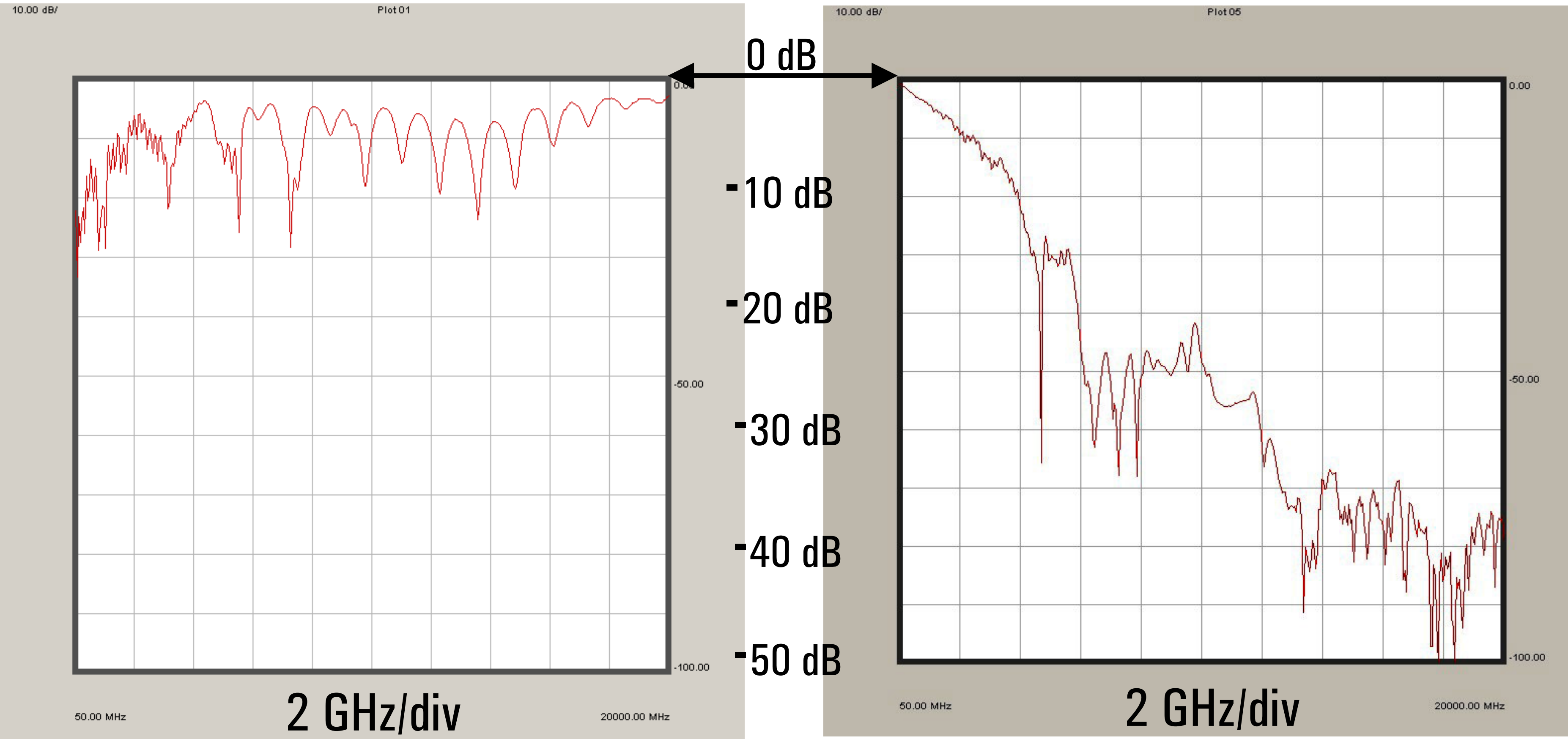
$S_{31} = S_{13}$: near end cross talk

$S_{41} = S_{14}$: far end cross talk

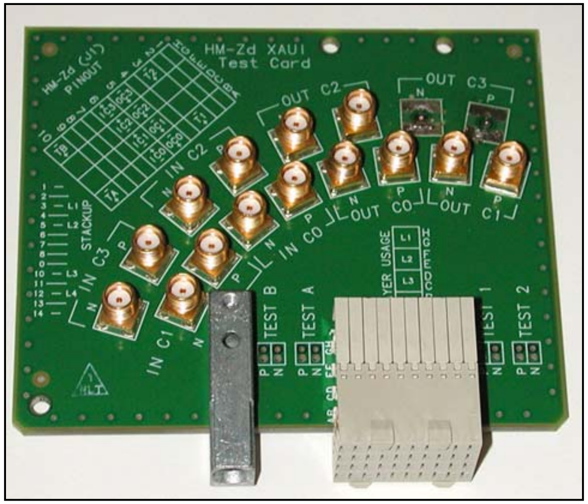
Single-ended Return Loss and Insertion Loss: 26 inch channel length

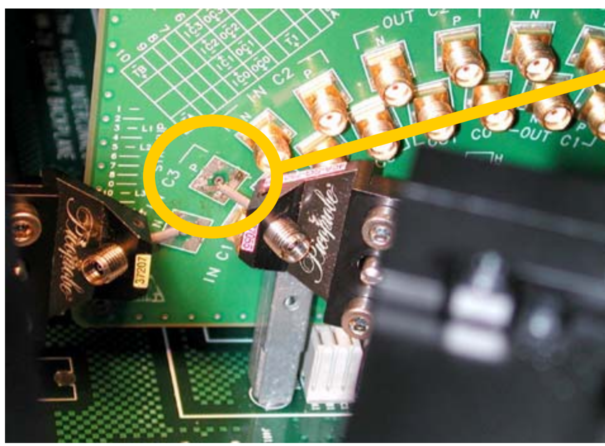
Input Single-ended Return Loss S11

Input Single-ended Insertion Loss S21

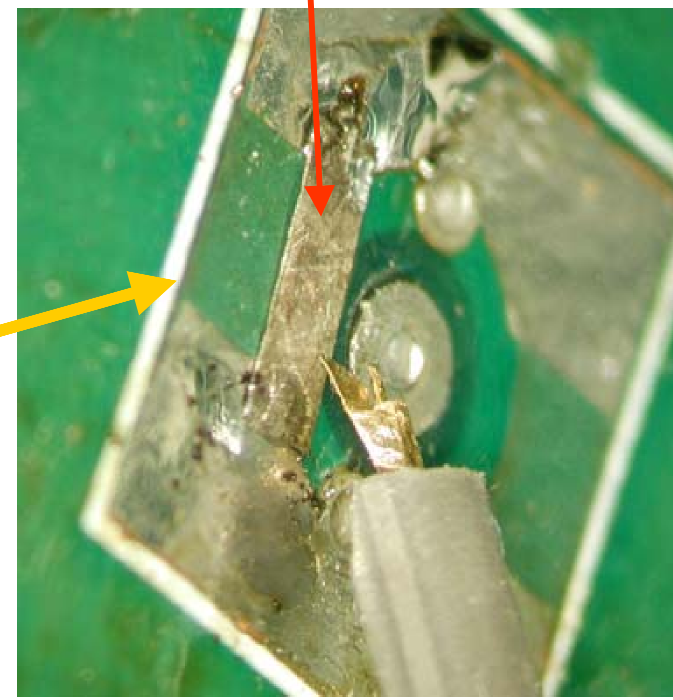


Microprobing on SMA Pads

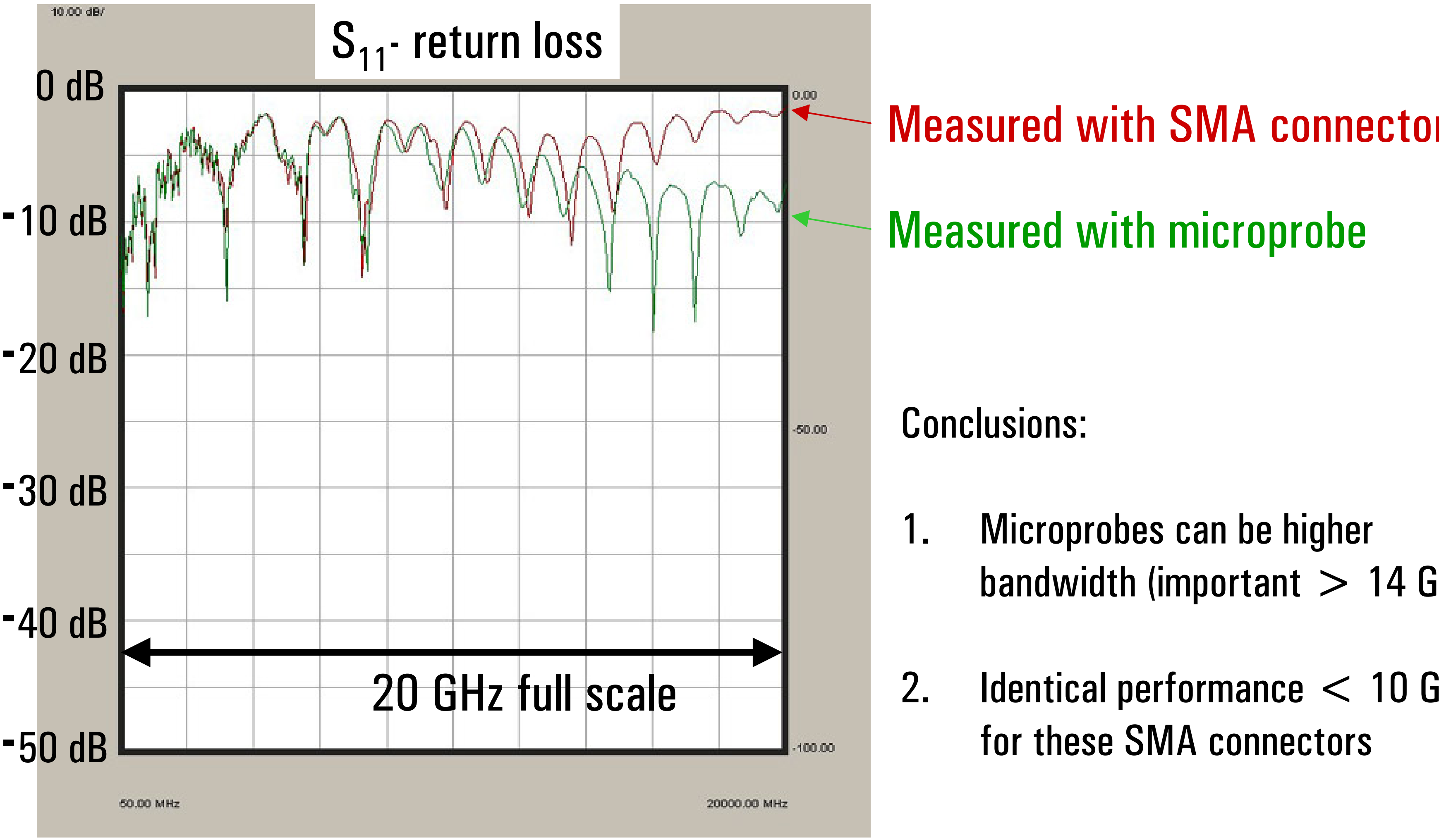




Added ground pad



Bandwidth Limit of SMA vs. Microprobes



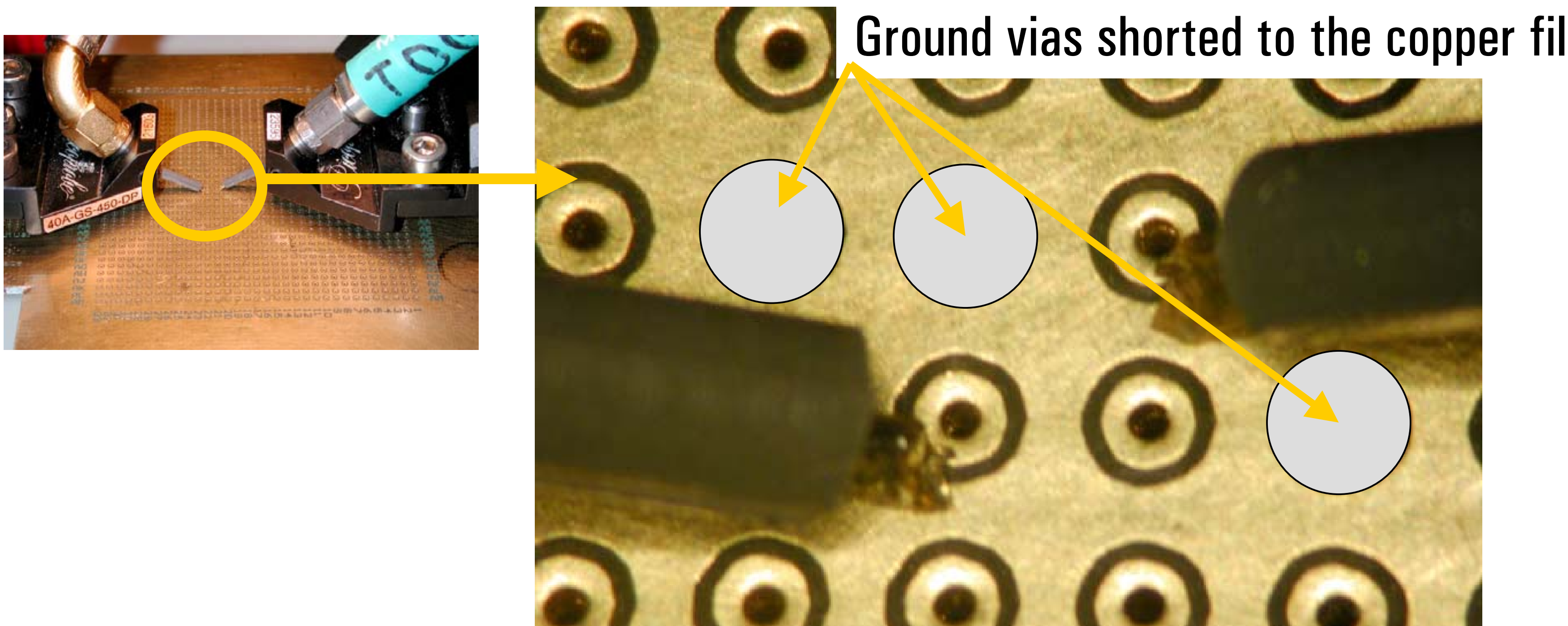
Conclusions:

1. Microprobes can be higher bandwidth (important > 14 GHz)

2. Identical performance < 10 GHz for these SMA connectors

Design for Test (DFT): Optimized Pad Design for Micro-probing

- Any signal via can be used as a probe point
- Use a “copper fill” around the signal via with immediate connection to all adjacent ground vias
- Every board should be designed with pads for optional microprobing- no impact on function



Microprobing vs. SMA Connectors

	Strengths	Weaknesses
SMA Connectors	• No additional fixturing to VNA required • Easy to use • Mechanically robust	• Can’t use on functional boards- loads the line too much • Limited density
Micro Probes	• Can use on any signal lines • No constraints on how many or where • Can be used on functional board • Important for active probing	• Probe station required • Probes can be damaged

Two Important Transformations Facilitate First Order Analysis

- From single-ended S-parameters to differential S-parameters
- From frequency domain to time domain

4 Port Balanced Measurements: Frequency and Time Domain

Single-ended

1 ——— 2

3 ——— 4

(and their return paths!)

Differential

Diff pair port 1 ═══ Diff pair port 2

(and their return paths!)

Single-ended: Stimulus / Response

Response \ Stimulus				
	S_{11}	S_{12}	S_{13}	S_{14}
	S_{21}	S_{22}	S_{23}	S_{24}
	S_{31}	S_{32}	S_{33}	S_{34}
	S_{41}	S_{42}	S_{43}	S_{44}

Differential: Stimulus / Response

Response		Stimulus: Differential Signal		Stimulus: Common Signal	
		Port 1	**Port 2**	**Port 1**	**Port 2**
Differential Signal	Port 1	S_{DD11}	S_{DD12}	S_{DC11}	S_{DC12}
Differential Signal	Port 2	S_{DD21}	S_{DD22}	S_{DC21}	S_{DC22}
Common Signal	Port 1	S_{CD11}	S_{CD12}	S_{CC11}	S_{CC12}
Common Signal	Port 2	S_{CD21}	S_{CD22}	S_{CC21}	S_{CC22}

The Meaning of the Quadrants

Differential in, differential out:
Behavior of differential signals

Common in, differential out:
Behavior of mode conversion

			Stimulus			
			Differential Signal		Common Signal	
			Port 1	Port 2	Port 1	Port 2
Response	Differential Signal	Port 1	S_{DD11}	S_{DD12}	S_{DC11}	S_{DC12}
		Port 2	S_{DD21}	S_{DD22}	S_{DC21}	S_{DC22}
	Common Signal	Port 1	S_{CD11}	S_{CD12}	S_{CC11}	S_{CC12}
		Port 2	S_{CD21}	S_{CD22}	S_{CC21}	S_{CC22}

Differential in, common out:
Behavior of mode conversion

Common in, common out:
Behavior of common signals

Important Performance Terms

Diff pair port 1

Diff pair port 2

(and their return paths!)

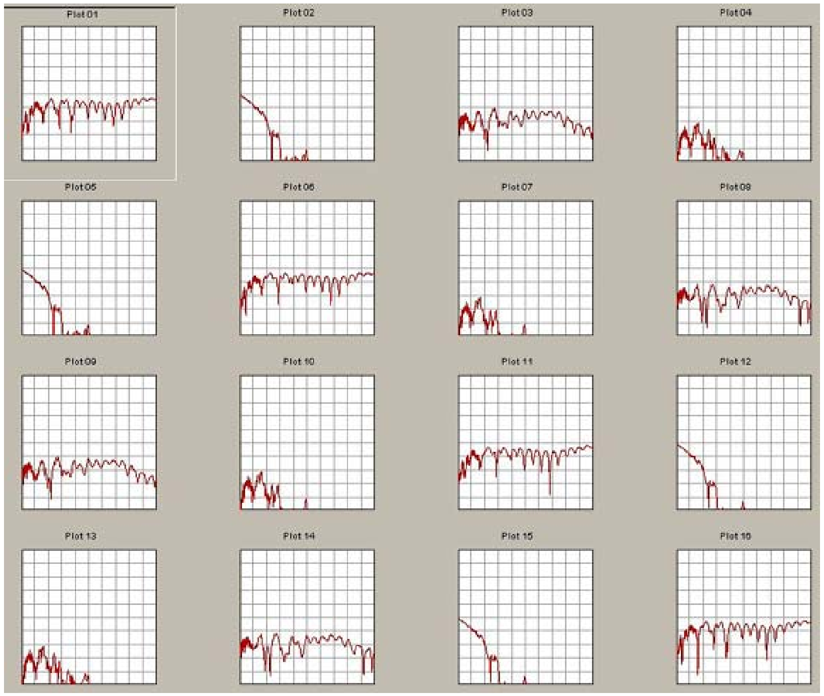
Stimulus

Response		Differential Signal, Port 1	Differential Signal, Port 2	Common Signal, Port 1	Common Signal, Port 2
Differential Signal	Port 1	S_{DD11}	S_{DD12}	S_{DC11}	S_{DC12}
Differential Signal	Port 2	S_{DD21}	S_{DD22}	S_{DC21}	S_{DC22}
Common Signal	Port 1	S_{CD11}	S_{CD12}	S_{CC11}	S_{CC12}
Common Signal	Port 2	S_{CD21}	S_{CD22}	S_{CC21}	S_{CC22}

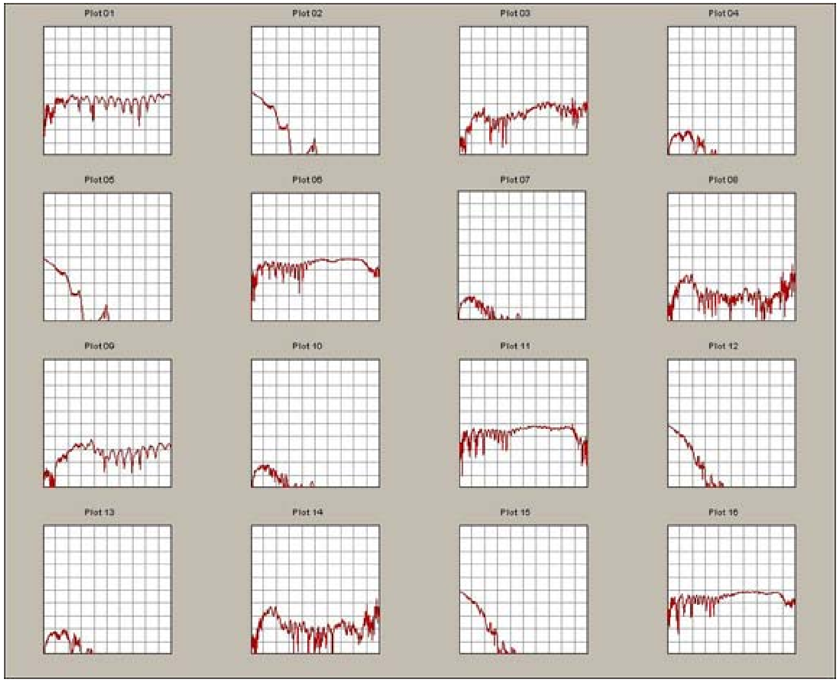
S_{DD11}	differential impedance profile
S_{DD21}	Signal quality of differential signal, time delay of differential signal
S_{CD21}	Conversion of differential signal to common signal in transmission (emissions)
S_{DC21}	Conversion of common signal to differential signal in transmission (susceptibility)
S_{CC11}	Common impedance profile
S_{CC21}	Signal quality of the common signal, time delay of common signal

Single-ended to Differential S-parameters

Single-ended S-parameters

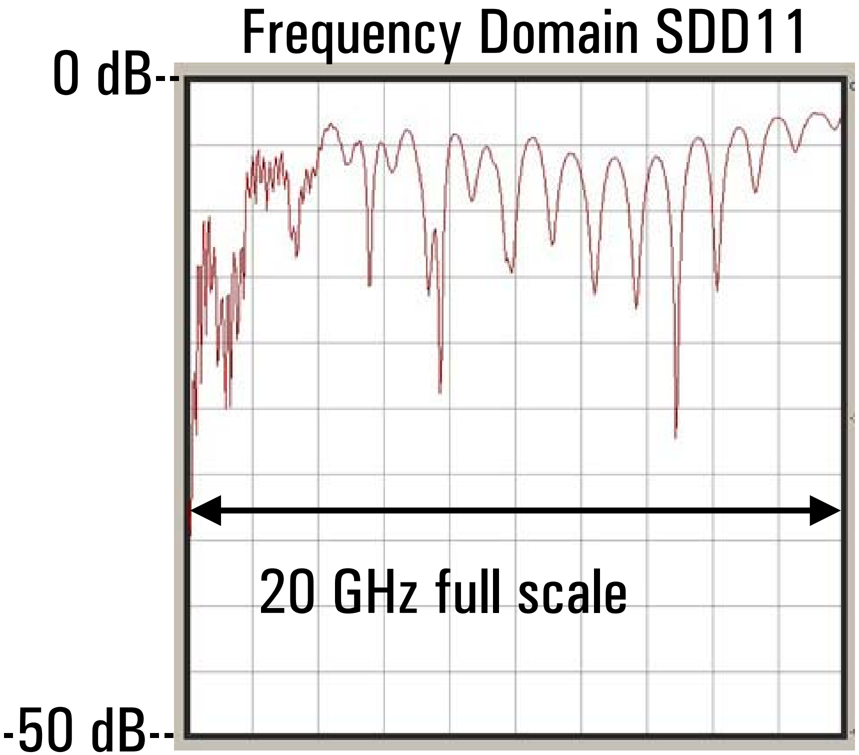


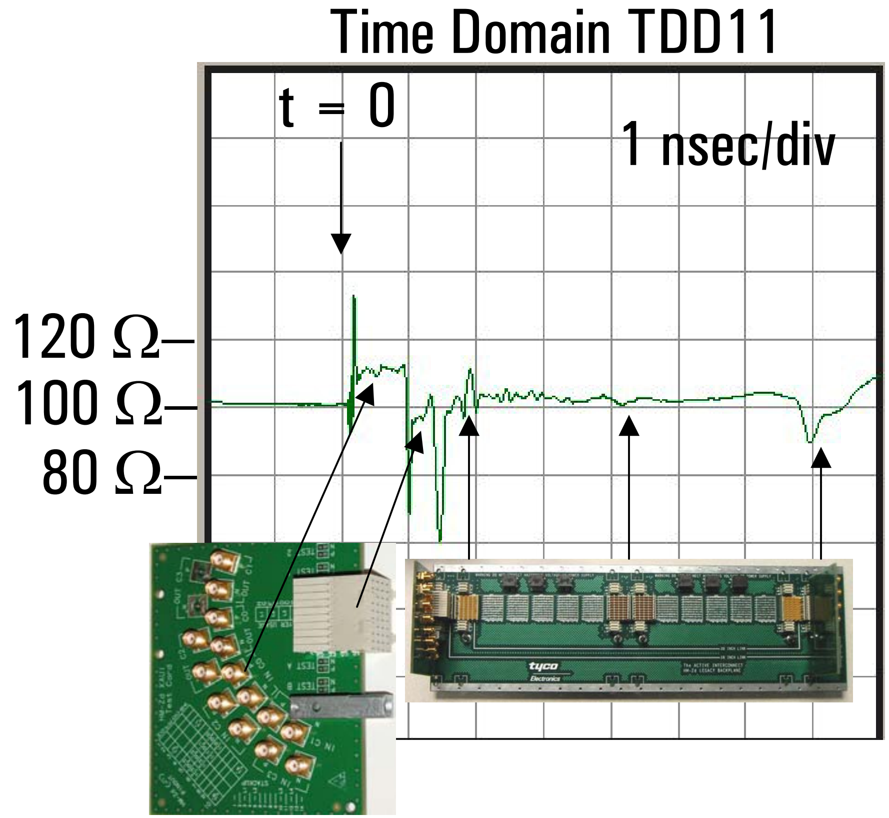
Differential S-parameters



Note: One measurement with Physical Layer Test System yields above information

Differential Return Loss & Reflection Coefficient





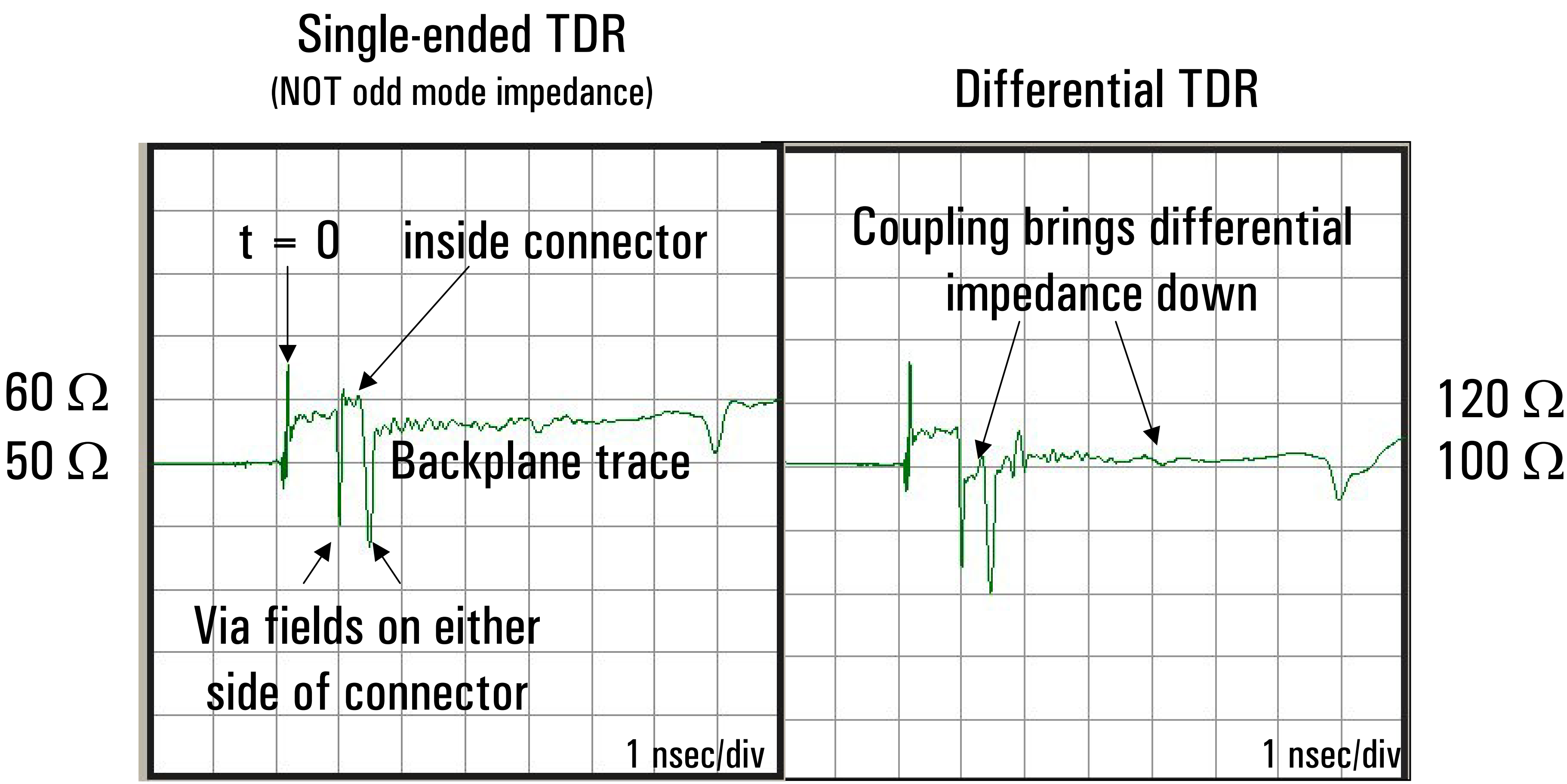
<u>Conclusions</u>

-Connectors create large impedance discontinuity

-Daughter card differential impedance is 110 Ω

-Backplane differential impedance is 102 Ω

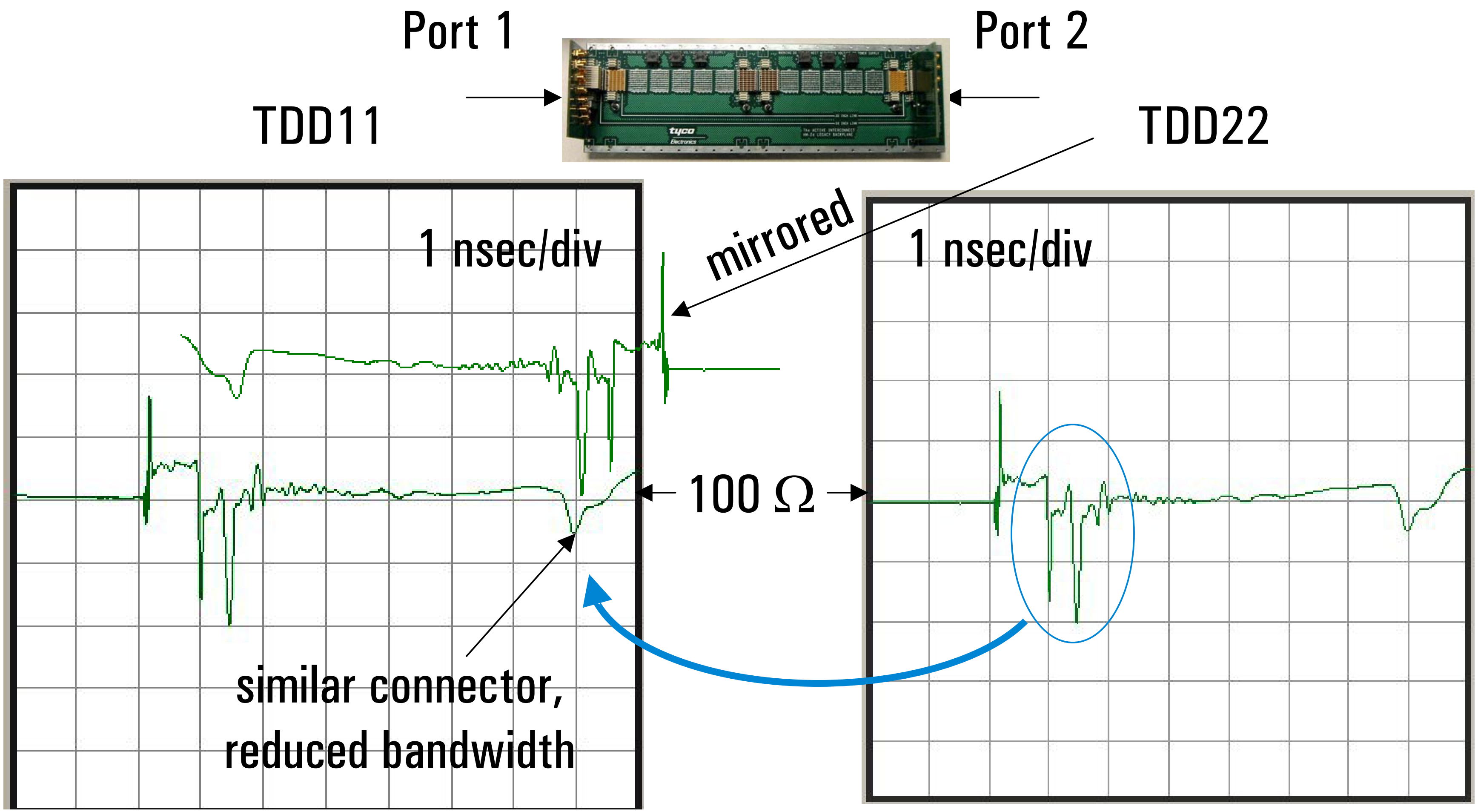
Single-ended and Differential TDR



Important Design Feedback

- Designing for 50 Ohm single ended line is not the same as a 100 Ohm differential line.
- Characterizing with single ended TDR will not measure differential impedance.
- Design the daughter cards with as much care as the backplane.
- Most discontinuities from connectors are not from the connectors- they are from the via fields.
- Optimizing connectors is all about optimizing the circuit board via field layout.
- Design for test: add copper fills for microprobing

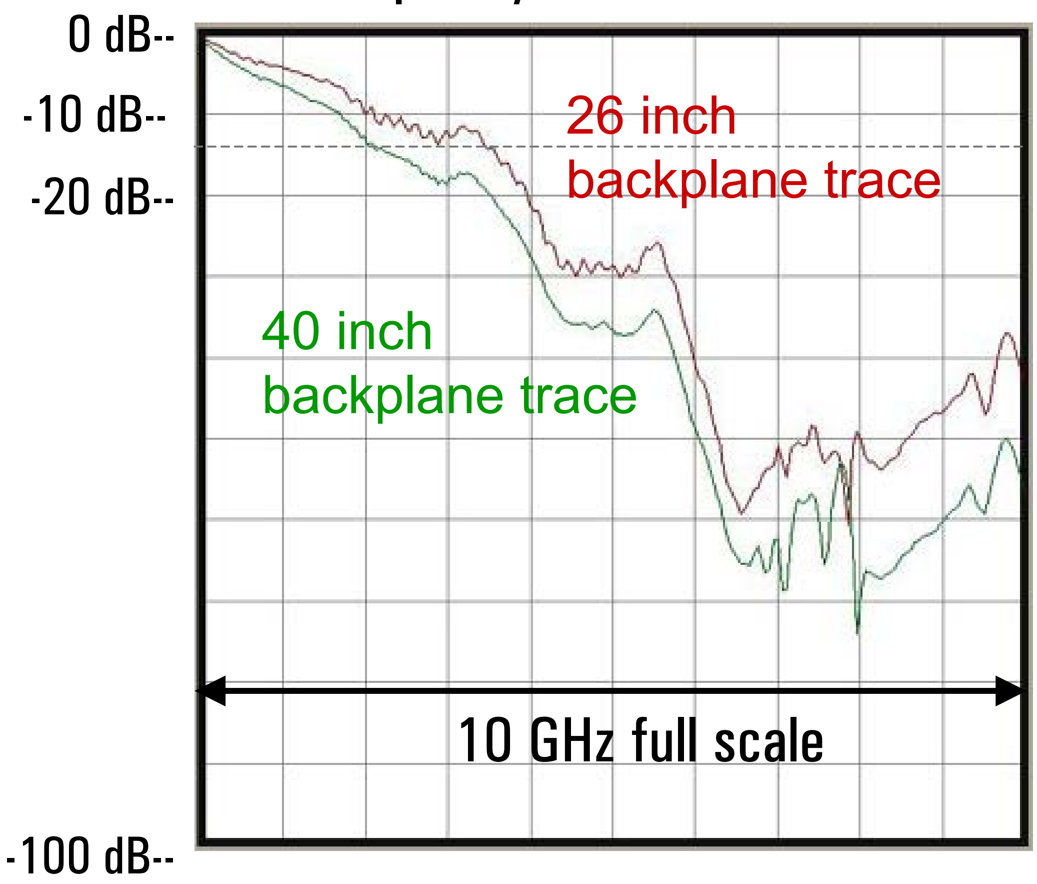
Differential TDR from Both Ends



Differential Transmitted Signal SDD21

- Conclusions:
  - Measurement system bandwidth > 40 GHz
  - 26 inch traces have a 15 dB BW ~ 3.5 GHz
  - 40 inch traces have a 15 dB BW ~ 2 GHz

Frequency Domain SDD21



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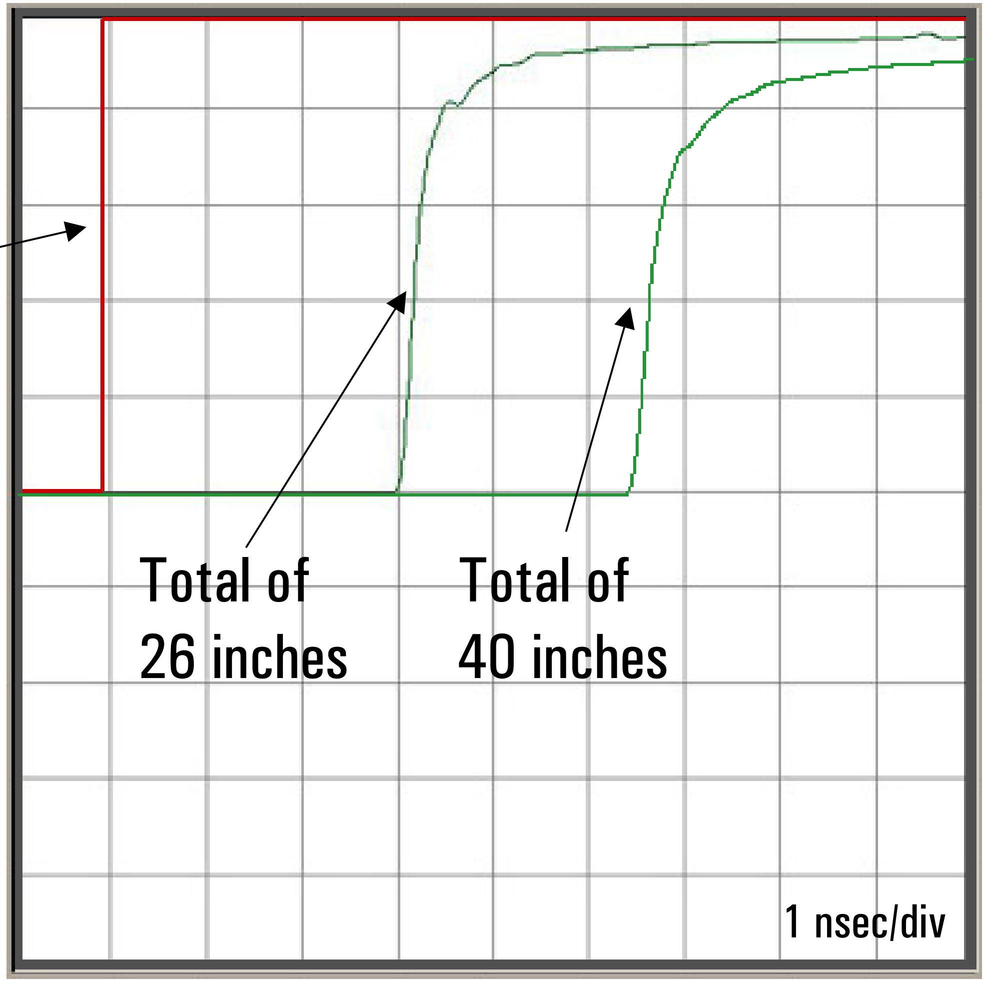
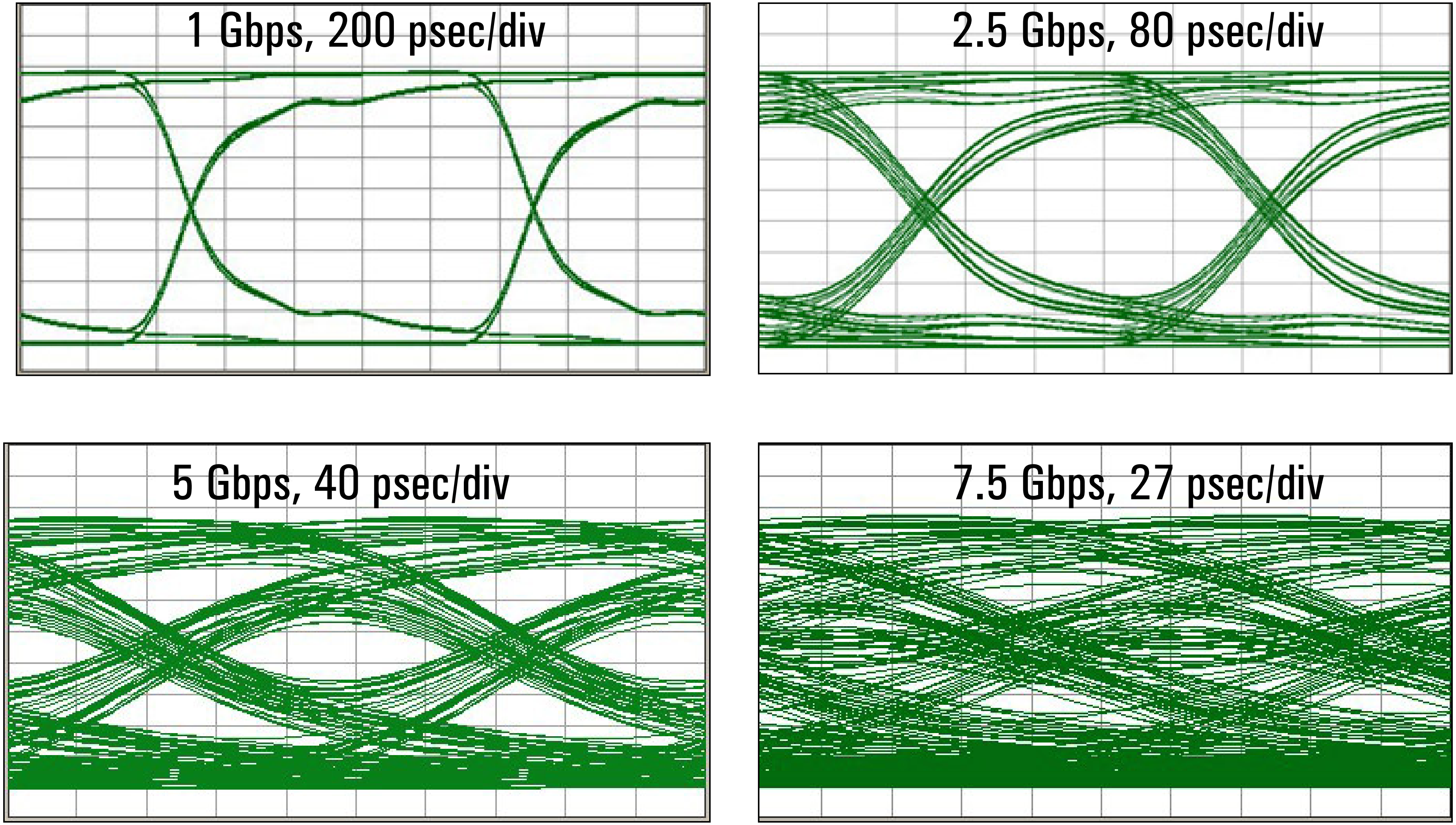
Differential Transmitted Signal: Time Domain TDD21

40 GHz bandwidth, ~ 20 psec input rise time



Eye Diagrams: 26 inch Channel



Non-ideal Differential Signaling: Mode Conversion

- Anything that affects one line and not the other will convert differential signal into common signal
- Drive is asymmetrical between channels
  - skew
  - output impedance and launched voltage
- Signal environment in interconnect is asymmetrical
  - different characteristic impedance in each leg
  - length is different
  - loading from connectors, jags, pads, ground planes

Real problem of common signal is EMI from <u>unshielded</u> twisted pair

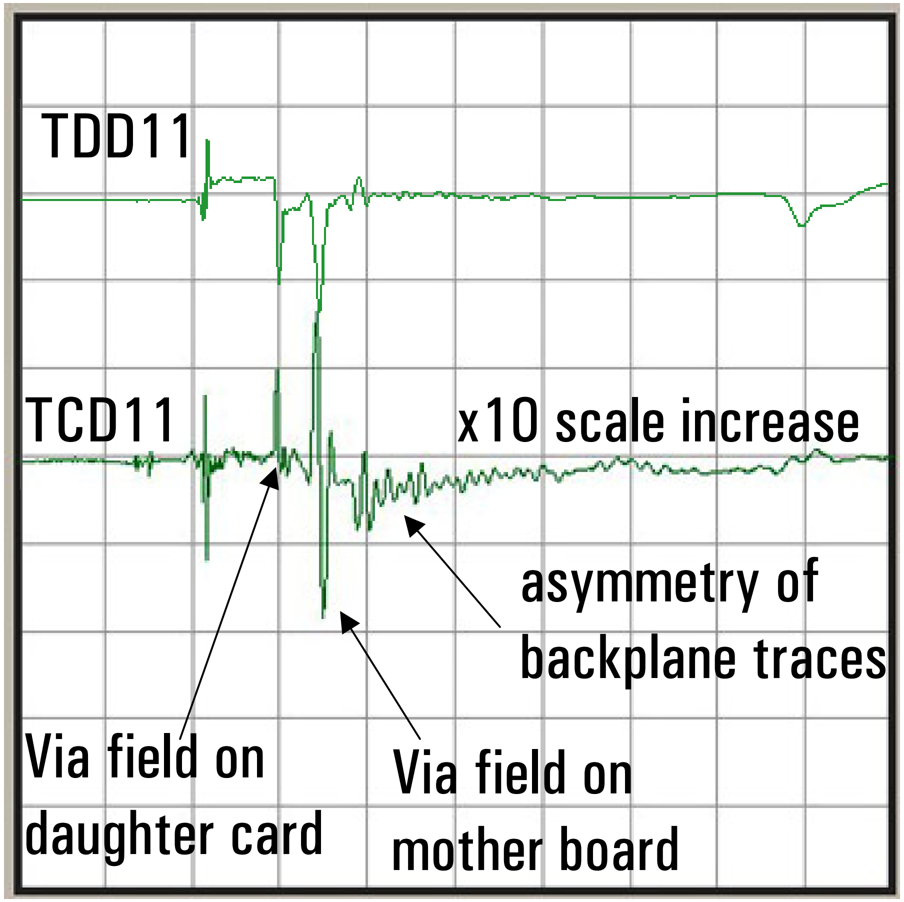
Differential Signal Input → Common Signal Output

26 inch channel length

~ 7% of differential signal amplitude converted to common signal

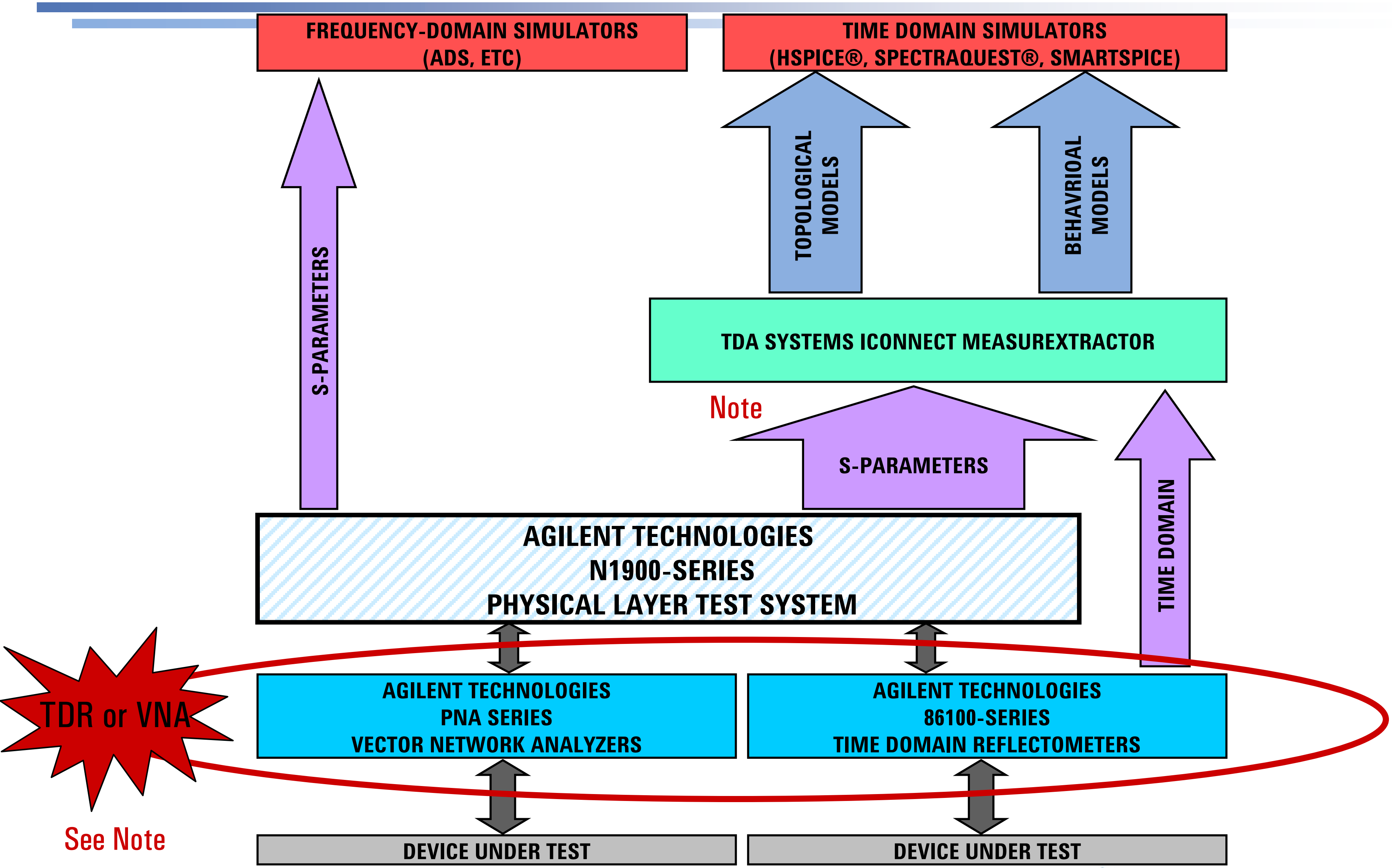
May be a problem if it were on CAT5 twisted pair

Where did the Conversion Happen?



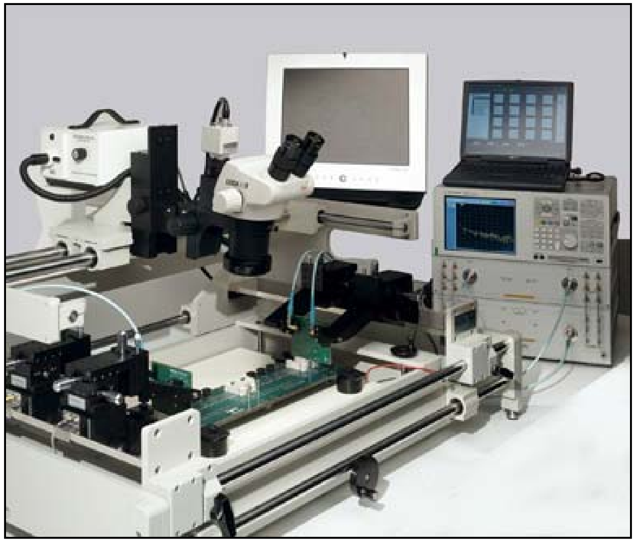
Conclusion: most mode conversion happens in the via fields!

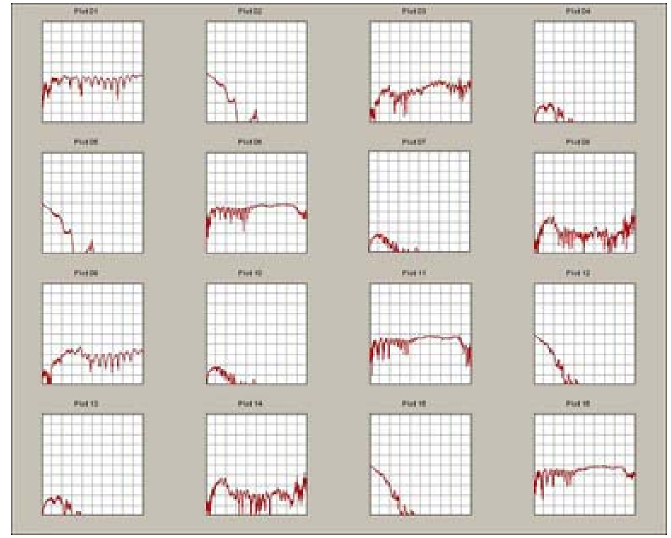
Measurement and Model Extraction

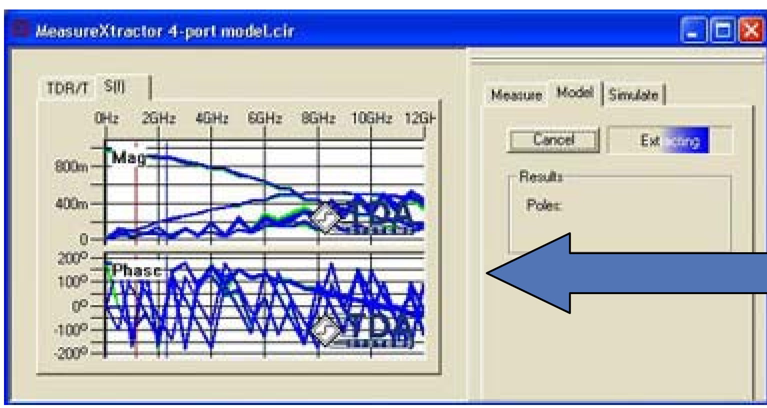


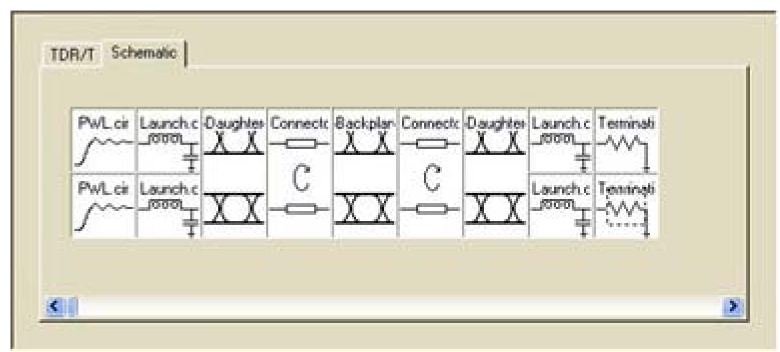
Note: TDR is *NEW* measurement engine for PLTS v1.2

Modeling Example with PLTS & IConnect









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Conclusions

- Differential pairs will proliferate
- Differential characterization requires
  - microprobes
  - probe station
  - 4 port VNA
  - Analysis software
- Absolutely everything you ever wanted to know about the performance of a differential pair is contained in the 4 port balanced S parameters- displayed in either the frequency or time domain

Technical Information Resources

- Visit *www.gigatest.com* *for..*
  - More than 100 application notes on high speed design
  - Schedule of signal integrity short courses
  - High-bandwidth measurement and modeling services
  - Complete signal integrity characterization systems

- Visit *www.agilent.com/find/plts* *for..*
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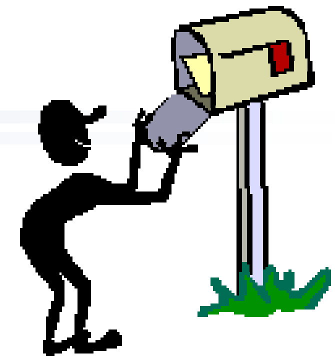

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